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10/762,864	01/21/2004	Wilson Wong	174/295	5928

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FOTAKIS, ARISTOCRATIS	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/762,864	WONG ET AL.	
	Examiner	Art Unit	
	ARISTOCRATIS FOTAKIS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/30/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3 - 8, 10 - 12, 14 - 16, 20 - 22, 24, 26 - 28, 30, 32 - 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3 - 8, 10 - 12, 14 - 16, 20 - 22, 24, 26 - 28, 30, 32 - 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3 – 7, 26, 33, 38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki (US 20040071205) in view of WinSLAC Software User's Guide (1999) and further in view of Solution Brief 41 ("FIR Compiler MegaCore Function", Altera Corporation, June 1999, ver.1).

Re claims 1, 26, 33, 38 and 41, Gorecki teaches of a circuitry (transceiver, Fig.4) for adaptively equalizing a data signal, the circuitry (Abstract) comprising: equalization implementation circuitry that includes a selectable tap parameter (*positioning of taps, pulse duration of taps, tap coefficients*), wherein the equalization implementation circuitry operates on the data signal (Paragraph 0042, 0043); programmable circuitry that is programmed by configuration data with a first value corresponding to a first tap parameter (*user*, Paragraph 0046); processing circuitry that computes a second value corresponding to a second tap parameter (*adaptive algorithm*, Paragraph 0044 – 0045); the user or system may select between the first and second numbers as the selectable number of taps selecting one of the first and second values only once (*initialization or*

start-up, Paragraph 0112). However, Gorecki does not specifically teach of the selection circuitry in a receiver circuitry based on a control signal selecting one of the first and second values and the number of taps being a tap parameter that is programmed or processed.

WinSLAC Software User's Guide discloses of equalization for both receive and transmit paths (page 4-15) controlled by user interface dialogs in the WinSLAC software (Page 3-5). The Guide further discloses of a selection circuitry based on a control signal (user interface) selecting one of a first value (*Calc or calculate*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19) and a second value (*Set*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19). However, WinSLAC Software User's Guide does not specifically show of the selection circuitry based on a control signal (user interface) selecting one of a first value that has been programmed and a second value that has been computed and that the number of taps being a tap parameter that is programmed or processed.

Solution Brief 41discloses of a FIR Compiler that identifies coefficients that match the frequency response specifies by the system. The coefficients can be read from a file or generated using the FIR compiler wizard. The function lets you specify the sample rate, the number of taps and cut-off frequencies. As you change the coefficient settings, you can view the frequency and the response of the filter dynamically (Pages 1 – 2, Fig.2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the equalization circuitry on the receiver so as to be able to monitor or compensate fast varying channel conditions. It would have been obvious to

one having ordinary skill in the art at the time the invention was made to have the selection circuitry select either the programmable circuitry or the processing circuitry controlled by the user to calculate or program tap parameters in order to provide a more flexible and user-defined system. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have had the two circuitries store the values into memory files before selection so as to avoid recalculations of the values. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have programmed or calculated the number of taps as an essential tap coefficient setting since it is required to know the exact number of taps before finding the tap coefficients.

Re claim 3, Gorecki teaches of the processing circuitry performing an algorithm to compute the second number (Paragraph 0045).

Re claim 4, Gorecki teaches of a memory coupled to the processor programmable logic device circuitry coupled to the processor circuitry and the memory (Paragraph 0112).

Re claims 5 - 6, Gorecki teaches of a printed circuit board comprising: a memory mounted on the printed circuit board and coupled to the programmable logic device circuitry (Paragraph 0112).

Re claim 7, Gorecki teaches of the printed circuit board further comprising: processor circuitry mounted on the printed circuit board and coupled to the programmable logic device circuitry (Paragraph 0112).

Claims 21 – 22, 30 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaynes et al (US US 2005/0047779) in view of WinSLAC Software User's Guide (1999) and further in view of Solution Brief 41 ("FIR Compiler MegaCore Function", Altera Corporation, June 1999, ver.1).

Re claims 22, 30 and 36, Jaynes teaches of a receiver circuitry ([0011]) for adaptively equalizing a data signal (Paragraph 0008, Figure) comprising: a first processing circuitry for computing an error signal using a selectable training pattern (#70, #72, Figure), wherein the first processing circuitry operates on the received data signal (Figure); programmable circuitry that is programmed by configuration data with a first training pattern and outputs the first training pattern (operator, Figure); training pattern circuitry that outputs a second training pattern (external process, Figure); and a first selection circuitry that receives the first training pattern and second training pattern; selects one of the first and second training patterns (external process or operator, Figure, Paragraph 0023) at the time the programmable circuitry is being programmed by configuration data (*user,* Paragraphs 0046, 0050, 0112), wherein the selection circuitry selects one of the first and second training patterns only once while the processing

circuitry operates the data signal (Paragraphs 0008, 0022 – 0023, 0026) and outputs the selected one of the first and second training patterns to the first processing circuitry..

However, Jaynes does not specifically teach of the selection circuitry receiving the first training pattern and second training pattern in parallel and selecting one of the training patterns based on a control signal from the programmable circuitry.

WinSLAC Software User's Guide discloses of equalization for both receive and transmit paths (page 4-15) controlled by user interface dialogs in the WinSLAC software (Page 3-5). The Guide further discloses of a selection circuitry based on a control signal (user interface) selecting one of a first value (*Calc or calculate*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19) and a second value (*Set*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19). However, WinSLAC Software User's Guide does not specifically disclose of the two values are in parallel before selection.

Solution Brief 41 discloses of a FIR Compiler that identifies coefficients that match the frequency response specifies by the system. The coefficients can be read from a file or generated using the FIR compiler wizard. The function lets you specify the sample rate, the number of taps and cut-off frequencies. As you change the coefficient settings, you can view the frequency and the response of the filter dynamically (Pages 1 – 2, Fig.2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the selection circuitry controlled by the user to select between a processed value and a programmers value in order to provide a more flexible and user-defined system. It would have been obvious to one having ordinary skill in the

art at the time the invention was made to have had the two circuitries store the values into memory files before selection so as to avoid recalculations of the values.

Re claim 21, Jaynes teaches of the first processing circuitry performing an algorithm to compute the error signal using a training pattern (*the error generator is a processor*, Paragraph 0015).

Claims 20, 40 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaynes, WinSLAC Software User's Guide and Solution Brief 41 in view of Hillery (US 6,178,201).

Re claims 40 and 44, Jaynes, WinSLAC Software User's Guide and Solution Brief 41 disclose all the limitations of claims 22 and 30 as well as Jaynes teaching of equalization implementation circuitry (#30) responsive to an error signal (#70), wherein the equalization implementation circuitry operates on the received data signal. As discussed above, Jaynes, WinSLAC Software User's Guide and Solution Brief 41 teach of wherein a processing circuitry receives the selected one of the first and second training patterns and computes the first error signal using the selected training pattern and outputs the first error signal. Jaynes further teaches of the processing circuitry can also compute a second decision directed error signal using a training pattern (#81) and outputs the second error signal. However, Jaynes does not specifically disclose of a separate (second) processing circuitry that computes a second decision directed error

signal using a training pattern and outputs the second error signal in parallel with the first error signal; and second selection circuitry that: receives a second control signal from the programmable circuitry, the first error signal and the second error signal in parallel; selects, based on the second control signal, one of the first and second error signals; and outputs the selected one of the first and second error signals to the equalization implementation circuitry, wherein the equalization implementation circuitry is responsive to the selected one of the first and second error signals.

Hillery teaches of a receiver circuitry for adaptively equalizing a data signal (Abstract) comprising: equalization implementation circuitry responsive to an error signal (Fig.1), wherein the equalization implementation circuitry operates on the received data signal (#22, Fig.1); first processing circuitry for computing a first decision directed error signal (#40, Fig.1, Col 3, Lines 54 – 67); second processing circuitry for computing a second error (#38, Fig.1, Col 3, Lines 38 – 50); and selection circuitry (#36, Fig.1) for selecting one of the first and second error signals as the error signal (Col 3, Lines 30 – 37), and outputs the selected one of the first and second error signals to the equalization implementation circuitry (#30), wherein the equalization implementation circuitry is responsive to the selected one of the first and second error signals (Fig.1). However, Hillery does not teach of the selector selecting based on a second control signal from the programmable circuitry.

WinSLAC Software User's Guide discloses of equalization for both receive and transmit paths (page 4-15) controlled by user interface dialogs in the WinSLAC software (Page 3-5). The Guide further discloses of a selection circuitry based on a control signal

(user interface) selecting one of a first value (*Calc or calculate*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19) and a second value (*Set*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have had two processing circuitries to generate the error signals so as to speed up the adaptation of the equalizer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the selection circuitry controlled by the user to select between a first value and a secondvalue in order to provide a more flexible and user-defined system.

Re claim 20, Hillery teaches of wherein the second processing circuitry performs an algorithm to compute the first second decision directed error signal (LMS, Col 3, Lines 50 - 65).

Claims 8 – 11, 24, 27, 32, 34, 37, 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki in view of Lu (US 6,275,836) and further in view of WinSLAC Software User's Guide (1999) and further in view of Solution Brief 41.

Re claims 8, 10, 27, 34, 39 and 42, Gorecki teaches of a circuitry (transceiver, Fig.4) for adaptively equalizing a data signal comprising: equalization implementation circuitry for adjusting or controlling the spacing of the taps (Paragraph 0043), wherein the equalization implementation circuitry operates on the data signal; programmable

circuitry for adjusting or controlling the spacing of the taps programmed by configuration data (*user,* Paragraphs 0046, 0050, 0112); processing circuitry for adjusting or controlling the spacing of the taps (Paragraph 0044 – 0045); the programmable circuitry or the processing circuitry may generate one of the tap spacing (Paragraph 0112) only once (*initialization or start-up,* Paragraph 0112), while the equalization implementation circuitry operates on the data signal (Paragraph 0112 – 0116). However, Gorecki does not teach of a programmable circuitry and processing circuitry for allowing a first selection between integer spacing and fractional spacing to be specified as well as the selection circuitry selecting either the output of the programmable circuitry or the processing circuitry but the equalization effects performed by either one of the two circuitries. However, Gorecki does not specifically teach of the selection circuitry in a receiver circuitry based on a control signal selecting one of the first and second values.

Lu teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract, Fig.3) comprising: equalization implementation circuitry including taps (interpolation filter) having a selected one of integer spacing and fractional spacing relative to the symbol rate of the data signal (Abstract, Lines 1 – 13, Fig.3); processing circuitry (#74, Fig.3) for computing a (second) selection (#76a, #76b, Fig.3) between integer spacing and fractional spacing (Abstract, Lines 9 – 13, Fig.3 and Col 7, Lines 17 – 29).

WinSLAC Software User's Guide discloses of equalization for both receive and transmit paths (page 4-15) controlled by user interface dialogs in the WinSLAC software

(Page 3-5). The Guide further discloses of a selection circuitry based on a control signal (user interface) selecting one of a first value (*Calc or calculate*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19) and a second value (*Set*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19). However, WinSLAC Software User's Guide does not specifically show of the selection circuitry based on a control signal (user interface) selecting one of a first value that has been programmed and a second value that has been computed.

Solution Brief 41 discloses of a FIR Compiler that identifies coefficients that match the frequency response specifies by the system. The coefficients can be read from a file or generated using the FIR compiler wizard. The function lets you specify the sample rate, the number of taps and cut-off frequencies. As you change the coefficient settings, you can view the frequency and the response of the filter dynamically (Pages 1 – 2, Fig.2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided the option to the user to choose between a fixed or fractional spacing depending on the incoming sampling rate for a good equalizer performance. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the selection circuitry selecting either the output of the programmable circuitry or the processing circuitry controlled by the user in order to provide a more flexible and user-defined system. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have had the two circuitries store the values into memory files before selection so as to avoid recalculations of the values. It would have been obvious to one having ordinary skill in

the art at the time the invention was made to have the equalization circuitry on the receiver so as to be able to monitor or compensate fast varying channel conditions.

Re claim 11, Gorecki, Lu, WinSLAC Software User's Guide and Solution Brief 41 teach of all the limitations of claim 8. Lu teaches of the fractional spacing is a selectable fraction of the symbol period (1/fs, sampling rate fs, Col 7, Lines 48 – 62), wherein the first selection can include a programmably specified first fraction, and wherein the second selection can include a processing-circuitry-computed second fraction (see claim rejection above).

Re claims 24, 32 and 37 Gorecki, Lu, WinSLAC Software User's Guide and Solution Brief 41 teach of a receiver circuitry for adaptively equalizing a data signal as discussed above in claims 8 – 11, comprising: equalization implementation circuitry, in the receiver circuitry, having at least one sampling point with a selectable location relative to a bit period of the received signal (*The symbol period of the tap spacing's is the inverse of the sampling frequency. Changing the tap spacing (as taught by Gorecki) will change the location of the sampling points*), wherein the equalization implementation circuitry operates on the data signal; programmable circuitry that is programmed by configuration data with a first value corresponding to a first location of the sampling point and outputs the first value and a control signal; processing circuitry that computes a second value corresponding to a second location of the sampling point and outputs the second value in parallel with the first value; and selection circuitry that:

receives the control signal from the programmable circuitry, the first value and the second value in parallel (*receiving two values in parallel and selecting only one as disclosed by WinSLAC Software User's Guide*); selects, based on the control signal, one of the first and second values at the time the programmable circuitry is being programmed by the configuration data, wherein the selection circuitry selects one of the first and second values only once, while the equalization implementation circuitry operates on the data signal; and outputs the selected one of the first and second values to the equalization implementation circuitry, wherein the location of the at least one sampling point of the equalization implementation circuitry corresponds to the selected one of the first and second values.

Claims 12, 14 – 16, 28, 35 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pederson et al (US 2006/0114979) in view of WinSLAC Software User's Guide (1999) and further in view of Solution Brief 41 ("FIR Compiler MegaCore Function", Altera Corporation, June 1999, ver.1).

Re claims 12, 28 and 35, Pederson teaches of circuitry for adaptively equalizing a data signal, the circuitry comprising: equalization implementation circuitry that includes at least one selectable coefficient value (FCS, Fig.6); first processing circuitry for computing the coefficient value (UPS) using a selectable starting value (iFCS), wherein the coefficient value (FCS) is different from the starting value (iFCS); programmable circuitry that is programmed by configuration data with a first starting

value and outputs the first starting value (Paragraph 0104, Lines 6- 8); second processing circuitry that computes a second starting value and outputs the second starting value (algorithm, Paragraph 0104, Lines 4 - 6); selects one of the first and second starting values (Paragraph 0104), only once (initial values); and outputs the selected one of the first and second starting values to the first processing circuitry (UPS), wherein the selectable starting value of the first processing circuitry corresponds to the selected one of the first and second values (Paragraph 0102 - 0105, Fig.6b). However, Pederson does not specifically of the programmable circuitry outputting a control signal used to select one of the two parallel values in a receiver.

WinSLAC Software User's Guide discloses of equalization for both receive and transmit paths (page 4-15) controlled by user interface dialogs in the WinSLAC software (Page 3-5). The Guide further discloses of a selection circuitry based on a control signal (user interface) selecting one of a first value (*Calc or calculate*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19) and a second value (*Set*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19). However, WinSLAC Software User's Guide does not specifically show of the selection circuitry based on a control signal (user interface) selecting one of a first value that has been programmed and a second value that has been computed in parallel.

Solution Brief 41discloses of a FIR Compiler that identifies coefficients that match the frequency response specifies by the system. The coefficients can be read from a file or generated using the FIR compiler wizard. The function lets you specify the sample rate, the number of taps and cut-off frequencies. As you change the coefficient

settings, you can view the frequency and the response of the filter dynamically (Pages 1 – 2, Fig.2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the equalization circuitry on the receiver so as to be able to monitor or compensate fast varying channel conditions. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the selection circuitry select either the programmable circuitry or the processing circuitry controlled by the user to calculate or program tap parameters in order to provide a more flexible and user-defined system. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have had the two circuitries store the values into memory files before selection so as to avoid recalculations of the values.

Re claim 14, Pederson teaches of wherein the first processing circuitry performs an algorithm to compute the coefficient value (Abstract).

Re claim 15, Pederson teaches of wherein the second processing circuitry performs an algorithm to compute the second starting value (Paragraph 0104).

Claims 16 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pederson, WinSLAC Software User's Guide (1999) and Solution Brief 41 in view of Gorecki.

Pederson, WinSLAC Software User's Guide (1999) and Solution Brief 41 teach all the limitations of claims 12 and 28 except of further comprising: further programmable circuitry for allowing selection between (I) operation of the first processing circuitry to fix on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced.

Gorecki teaches of selection between (1) operation of the first processing circuitry to fix (*adjust*) on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt (*control or vary*) the coefficient value even after satisfactory equalization has been produced (paragraphs 0047, 0058, 0062 – 0065 and 0070).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the user select between a fixed and continuous operation for the benefits of having a more flexible and user-defined system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 6:30 - 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aristocratis Fotakis/

Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611